IN THE SPECIFICATION:

Amend paragraph 27 as follows:

[0027] Layer 50, illustratively an insulator such as oxide or nitride (Si_3N_4), provides isolation between source 30 and gate 60 at the center of the Figure. As will be discussed below, gate 60 and the underlying layers are provided with a high degree of planarity, so that the thickness of layer 60 is highly uniform across the circuit, having a gate layer thickness within a thickness tolerance. The uniformity in thickness translates to a corresponding uniformity in channel length in the devices.

Amend paragraph 46 as shown:

[0046] Those skilled in the art will appreciate that current technology permits the gate layer to be formed with a thickness in the range of 5 - 200nm and a thickness tolerance of about 2% - 5%, three sigma. This provides a more uniform transistor channel length across a circuit than is practical with lithographic techniques.